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Compiler Construction

Lecture 22: Code generation

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Overview

- Instruction selection
- Register allocation (next lecture)



Where are we now?

- We have a fairly low-level view of the program, but
 - It features a memory model of infinite temporary variables
 - It isn't specific in terms of operations provided by the architecture
- These will be our last two topics
 - Selecting machine-specific operations
 - Mapping variables to memory locations

Low-level IR vs. machine level

• The instructions of a low-level IR are not the same as the ones of the target machine



Straight forward solution

Map every low-level IR to a fixed sequence of assembly instructions



- Disadvantages:
 - Lots of redundant operations
 - More memory traffic than necessary

Multiple possible alternatives

• Translate a [i+1] = b [j] using these operations

```
add r2, r1\leftarrow r1 = r1+r2mul c, r1\leftarrow r1 = r1*cload r2, r1\leftarrow r1 = *r2store r2, r1\leftarrow *r1 = r2movem r2, r1\leftarrow *r1 = *r2movex r3, r2, r1 \leftarrow *r1 = *(r2+r3)
```

General code generation steps

- Let us assume that everything is represented by 8-byte elements, and
 - Register r_a holds &a
 - Register r_b holds &b
 - Register r_i holds i
 - Register r_j holds j

a[i+1] = b[j] needs to

- Find address of b [j]
- Load b[j]
- Find address of a [i+1]
- Store into a [i+1]

One translation

- Address of b [j]
 - mulc 8, r_j
 - add r_j, r_b
- Load b[j]
 - load r_b,r1
- Address of a [i+1]
 - add 1,r_i
 - mulc 8, r_i
 - add r_i, r_a
- Store into a [i+1]
 - store r1, r_a



Another possible translation

- Address of b [j]
 - mulc 8, r_j
 - add r_j, r_b
- Address of a [i+1]
 - add 1,ri
 - mulc 8, r_i
 - add r_i, r_a
- Store into a [i+1]
 - movem r_b, r_a



One more translation

- Address of b [j]
 - mulc 8, r_j
- Address of a [i+1]
 - add 1,r_i
 - mulc 8, r₁ .
 - add r_i, r_a
- Store into a [i+1]

• movex r_j, r_b, r_a

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TAC

t2 = b + t1

t4 = i + 1

t5 = t4

*t6 = t3

t6 = a

t1

t3

j * 8

* 8

+ t5

Why should we care?

- Not all instructions are created equal
- Some complete in a clock cycle
- Others decompose into a sequence of steps, and take many cycles
- If we have a choice of translations, we'd like the one with the smallest sum of costs



Partial instructions aren't necessarily adjacent

- Address of b [j]
 - mulc 8, r_j
- Address of a [i+1]
 - add 1,r_i
 - mulc 8, r_1
 - add r_i, r_a
- Store into a [i+1]
 - movex r_j, r_b, r_a





Tree representation

• The 4 overall steps can be written as a tree





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Instructions can be tiles

• tile = subtree of a particular pattern





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Instructions can be tiles

• tile = subtree of a particular pattern





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Tiling

• An instruction selection covers the tree with disjoint tiles





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Tiling

• An instruction selection covers the tree with disjoint tiles





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Comparing the tilings

• Alternate tilings give different costs





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Better than trees

- If we let common sub-expressions be represented by the same node, the trees become *directed acyclic graphs* (DAGs)
- Separate labels and annotations
 - Label nodes with variables, constants or operators
 - Annotate nodes with variables that hold their value
 - Construct DAG from low-level IR



Basic approach

- For each instruction in a basic block
 - if it's "x = y op z"
 - find or create a node annotated y
 - find or create a node annotated z
 - find or create a node labeled op with operands y and z
 - remove annotation x from everywhere
 - add annotation x to the op node
 - if it's "x = y"
 - find or create a node annotated y
 - add annotation x to it







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